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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,372	08/06/2003	Richard W. Adkisson	200208997-1	1276

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/635,372	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/6/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10/635,372, 08/06/2003, which claims benefit of provisional US Application No. 60/469,180, filed 05/09/2003.

Claims 1-23 are presently under examination and still pending in the Application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification lacks enablement with respect to the claimed limitation "hot signal" recited in the independent claim 1, 10 and 17. Even though, the definition of a "hot signal" is well known in the art, which may imply an active or live signal while the main power is still on, in this case the specification fails to adequately describe the definition of the hot signal as applied to the claimed invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine

the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). In this case, the term "hot signal" in the claims is used by the claims to mean "an encoded signal during test", while the accepted meaning is "an active or live signal while the main power is still on." The term is indefinite because the specification does not clearly redefine the term. Therefore, for purpose of examination, the "hot signal" is given a broad interpretation to mean an encoded signal generated from a unit under test, when power is still on.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9, 16, 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Gates et al. (US Patent No. 6,311,303) issued: October 30, 2001.

Regarding independent Claim 1, Gates discloses methods and interfaces for facilitating testing or debugging of an integrated circuit containing a monitor port with trace bus, several circuit modules and a selection circuit for observing the internal signals for debugging the integrated circuit during the final stages of the integrated

circuit design and testing, (integrated circuits 100, 200, 300, as shown in Figs. 1-3, respectively), comprising:

A selection circuit (tri-state buffers 121 to 11N coupled to a trace select register 150) to select the set of signals from each module (111 to 11N) connected to bus 130 via the associated set of tri-state buffers 121 to 12N, according to expected usefulness of the signals during debugging of the module. The trace select register 150 provides the signals to enable or disable tri-buffers 121 to 12N and thereby select the module that drives internal signals onto bus 130 for output through the monitor port, Fig. 1. In an alternative embodiment of Fig. 2, a multiplexer 220 instead of the tri-state buffers is coupled to the trace select register 150 to select which of module 111 to 11N (i.e., which bus 231 to 23N) drives the output bus 230 of the monitor port.

A line decoder operating to decode the plurality of encoded state coverage signals, as described by Gates, "a decoder (not shown) attached to register 150 decodes the value in register 150 and generates signals that enable selected tri-state buffers 121 to 12N. Aside from the limitation that only one of modules 111 to 11N can drive a line of bus 130 at a time, the decoding of the value in register 150 can enable any combination of tri-state buffers from one or more sets of tri-state buffers 121 to 12N to select a desired combination of internal signals for output through the monitor port".

A capture circuit (host computer) for capturing the internal signals form the monitor port interface 340, which is connected to host interface 310 via a trace bus 345, selects the internal signals from within host adapter 300 for external monitoring on

output balls or pins of a monitor port, by. The monitor port interface 340 is generally for debugging of host adapter 300 during initial design and testing, Fig. 3.

Regarding Claims 9, 16, 23, tri-state buffers (1 to N), where N is a value 1 to N, including N=80.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-8,10-15 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gates et al. (US Patent No. 6,311,303) in view of Ricchetti et al. (US Patent No. 6,957,371).

Regarding independent Claims 10, 17, Gates discloses methods and interfaces for facilitating testing or debugging of an integrated circuit containing a monitor port with trace bus, several circuit modules and a selection circuit for observing the internal signals for debugging the integrated circuit during the final stages of the integrated circuit design and testing, (integrated circuits 100, 200, 300, as shown in Figs. 1-3, respectively), comprising:

With respect to claimed limitation of "encoding state coverage information generated when said logic design is under test", integrated circuit 100, Fig. 1, includes several circuit modules (111 to 11N), where each module receives (encoded data) input signals from input cells (not shown) and generate output signals that are useful for debugging integrated circuit 100 during the final stages of integrated circuit design and testing.

A selection circuit (tri-state buffers 121 to 11N coupled to a trace select register 150) to select the set of signals from each module (111 to 11N) connected to bus 130 via the associated set of tri-state buffers 121 to 12N, according to expected usefulness of the signals during debugging of the module. The trace select register 150 provides the signals to enable or disable tri-buffers 121 to 12N and thereby select the module that drives internal signals onto bus 130 for output through the monitor port, Fig. 1. In an alternative embodiment of Fig. 2, a multiplexer 220 instead of the tri-state buffers is coupled to the trace select register 150 to select which of module 111 to 11N (i.e., which bus 231 to 23N) drives the output bus 230 of the monitor port.

A line decoder operating to decode the plurality of encoded state coverage signals, as described by Gates, "a decoder (not shown) attached to register 150 decodes the value in register 150 and generates signals that enable selected tri-state buffers 121 to 12N. Aside from the limitation that only one of modules 111 to 11N can drive a line of bus 130 at a time, the decoding of the value in register 150 can enable any combination of tri-state buffers from one or more sets of tri-state buffers 121 to 12N to select a desired combination of internal signals for output through the monitor port".

A capture circuit (host computer) for capturing the internal signals form the monitor port interface 340, which is connected to host interface 310 via a trace bus 345, selects the internal signals from within host adapter 300 for external monitoring on output balls or pins of a monitor port, by. The monitor port interface 340 is generally for debugging of host adapter 300 during initial design and testing, Fig. 3.

Regarding Claims 2-8,10-15 and 17-22, Gates does not explicitly disclose generating an N-bit mask value stored in a register block for generating an N-bit output. In analogous art, Ricchetti et al. (US Patent No. 6,957,371) discloses a Parallel-To-Serial Conversion (PTSC) circuit 618, which provides Mask Data Out (MDO) signal to the Compare (CMP) circuit 612 to allow the system BIST controller 502 to mask one or more of the expected TDI data bits sent back from the UUT(s).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the masking feature as taught by Ricchetti, in the debugging circuitry of Gates. A person skilled in the art would have been motivated to mask such data, when the expected value for a bit of TDI data is indeterminate or unknown logic value. Accordingly, when the MDO signal is asserted in the serial data stream, this signal indicates to the CMP circuit 612 that the result of the corresponding TDO-EDO bit compare is to be ignored, in effect forcing the comparison of the bit to pass, thus saving testing time.

Conclusion

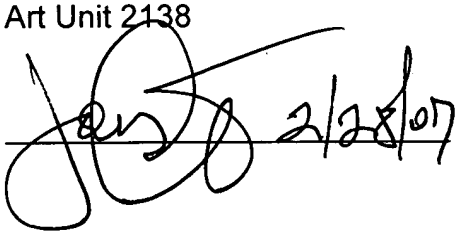
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



Date: 28 February 2007
Office Action: Non-Final Rejection

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